23. A method for translating physical memory cell coordinates of a memory device, said method comprising:

inputting a physical cell coordinate of a memory device; and

applying a set of displacement and mirror factors to said physical cell coordinate to translate said physical cell coordinate into a logical address.

24. The method in claim 23, wherein said logical address comprises an N- dimensional logical address, wherein N comprises a natural number.

A2

25. The method in claim 23, further comprising:

identifying repeatable memory cells of said memory device;

preparing a look up table for translating buffer coordinates of a reference memory cell of said repeatable memory cells;

displacing information from said look up table to correspond to said repeatable memory cells; and

modifying results of said displacing by a linear operation.

26. The method in claim 25, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

27. The method in claim 25, wherein said reference memory cell comprises a smallest repeatable memory cell.

28. The method in claim 27, further comprising:

identifying a first level of repeatable memory cells, having a size larger than said smallest repeatable memory cell;

identifying a second level of repeatable memory cells, having a size larger than said first level of repeatable memory cells; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

29. The method in claim 25, wherein said displacing and modifying comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

30. A method for translating physical memory cell coordinates of a memory device to logical addresses, said method comprising:

identifying repeatable memory cells of said memory device;

preparing a look up table for translating physical cell coordinates of said repeatable memory cells into logical addresses; and

displacing information from said look up table to correspond to said repeatable memory cells.

31. The method in claim 30, wherein said logical addresses comprise N-dimensional logical addresses, wherein N comprises a natural number.

32. The method in claim 30, further comprising modifying results of said displacing by a linear operation.

33. The method in claim 30, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

34. The method in claim 30, wherein said reference memory cell comprises a smallest repeatable memory cell.

35. The method in claim 34, further comprising:

identifying a first level of repeatable memory cells, having a size larger than said smallest repeatable memory cell;

identifying a second level of repeatable memory cells, having a size larger than said first level of repeatable memory cells; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

36. The method in claim 30, wherein said displacing comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

37. A method for translating physical memory cell coordinates of a memory device to logical addresses, said method comprising:

identifying repeatable memory cells of said memory device;

identifying a first level of said repeatable memory cells, said first level having a size larger than a smallest repeatable memory cell;

identifying a second level of said repeatable memory cells, said second level having a size larger than said first level of repeatable memory cells;

preparing a look up table for translating physical cell coordinates of said repeatable memory cells into logical addresses; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

38. The method in claim 37, wherein said logical addresses comprises N-dimensional logical addresses, wherein N comprises a natural number.

39. The method in claim 37, further comprising modifying results of said displacing by a linear operation.

40. The method in claim 37, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

41. The method in claim 37, wherein said displacing comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f'(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

42. A method for translating physical memory cell coordinates of a memory device, said method comprising:

inputting a physical cell coordinate of a memory device; and

applying a set of displacement and mirror factors to said physical cell coordinate to translate said physical cell coordinate into one of a logical address, an electrical address, and a structural address,

wherein said logical address, said electrical address, and said structural address comprise N- dimensional addresses, wherein N comprises a natural number.